

Unique Paper Code : 32341102

Name of the Paper : Computer System Architecture

Name of the Course : B.Sc. (H) Computer Science

Semester : I

Duration : 3 Hours

Maximum Marks: 75

**Instructions for the Candidates**

**Attempt Any Four Questions. All Questions Carry Equal Marks.**

Q1.

Given the Boolean function  $f(A, B, C, D) = \Sigma (1, 2, 3, 7, 8, 10)$  and don't-care conditions  $d(A, B, C, D) = \Sigma (0, 5, 6, 11, 15)$

- Obtain an optimized Boolean expression F in SOP form using Karnaugh map.
- Find complement of the optimized expression F using De-Morgan's Law.
- Draw the logic diagram of the original expression f and the optimized expression F. Compare the total number of gates for both.
- For the optimized expression F, show that  $F.F' = 0$  and  $F + F' = 1$
- Simplify the following expression using Boolean algebra:  $AB + A(CD + CD')$

Q2.

Perform following operations as directed (Use signed 2's complement representation for negative numbers):

- Convert  $(4433)_5$  to decimal and then to binary.
- Convert  $(5654)_8$  and  $(1199)_{12}$  to binary and then to Hexadecimal
- Add  $(6E)_{16}$  and  $(C5)_{16}$
- Subtract  $(7B)_{16}$  from  $(C4)_{16}$
- Give BCD representation of F3EA
- Add 679.6 and 536.8 in BCD
- Specify the value that will be assigned to interrupt flip-flop R in the following register transfer statement  
 $(T0 + T1 + T2) (IEN') (FGI') (FGO')$ :  $R \leftarrow ?$
- Explain briefly what will happen when the following micro instruction is executed:  
 If  $(AC(15) = 1)$  then  $S \leftarrow 0$

Q3.

- Write a program to evaluate the arithmetic expression:  $x = \frac{(B * C + A)}{B}$  using one address instructions.
- Assuming the three bit binary code for a register corresponds to the register number and the binary codes for microoperations supported by the processor are listed in Table 1, give the microinstruction that will be executed if the following 14-bit binary control words are specified to the processor:
  - 01001110010010
  - 01110001101011
  - 10100001110100

OPR SELECT	Operation
00000	Transfer
01011	OR
10010	ADD
10001	AND
10100	Complement

Table -1: Encoding of ALU operations

- Give the excitation table for a flip flop XY whose characteristic table is given as follows:

X	Y	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

- Draw a space-time diagram for a six-segment pipeline to process five tasks.

Q4.

- Consider the following snapshot of a memory to answer the questions that follow:

Memory	
402	800
.	
.	
.	
600	MODE    OPCODE
601	402
.	
.	
.	
800	90

A two word instruction being currently executed is stored at location 600 with its address field at location 601.

- Which addressing mode is being used if the value of operand is 90, 402 and 800 respectively?
- If the effective address obtained by using indexed register addressing mode is 902, what is the content of index register?
- What would be the value of program counter (PC) before and after the execution of the instructions:
  - if the OPCODE of the instruction is ADD?
  - if the OPCODE of the instruction is BUN?
- With reference to the basic computer, identify error(s) / explain why each of the following microoperations cannot be executed in a single clock pulse. Also, specify the correct sequence of microoperations that will perform the operation.
  - $TR \leftarrow M[PC]$
  - $M[AR] \leftarrow PC, PC \leftarrow AR + 1$
  - $M[AR] \leftarrow DR + 1$
  - $OUTR \leftarrow AC, FGO \leftarrow 1$

Q5.

- Show the construction of a 4 x 16 decoder using five 2 x 4 decoders with the help of a block diagram. Also give the truth table of the constructed decoder.
- Specify the number of bytes that can be stored in a 128K × 16 memory. How many address lines and data lines will be required for the specified memory unit? How many 256 x 8 memory chips will be needed to provide a memory capacity of 4096 x 16?
- Identify the type of following I/O interface commands:
  - Check to see if a printer is ready for printing
  - Skip to the beginning of a tape
  - Check for an error during an I/O transfer
  - Write a block of data onto a magnetic disk.

Q6.

- A computer uses a memory unit of 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an addressing mode field to specify one of the four addressing modes, an operation code, a register code part to specify one of the 128 registers and an address part. Calculate the number of bits in each part of the instruction and indicate them by drawing the instruction format.
- Which flip-flop will need to be disabled in case processor is not in a position to serve any interrupts? Which flags are checked to determine whether the source of interrupt is from an input device or an output device respectively?



Figure I. The Common Bus System

- Consider the common bus system of the basic computer depicted in Figure I. The control inputs given in Table II are active in the common bus system at a time instant  $t_0$ . Give register transfer statements to specify the register transfer(s) that will be executed during the next clock transition  $t_1$ .

	$S_2$	$S_1$	$S_0$	LD of register	Memory	Adder
I.	0	0	1	PC	-	-
II.	1	0	0	DR	Read	-
III.	0	1	1	AC	-	Add
IV.	1	1	1	TR	Read	-

Table II Control Inputs active in Common Bus System at time instant  $t_0$

- The following register transfer operations are to be executed in the common bus system (Figure 1). For each transfer, specify the binary value that must be applied to the selection inputs  $S_2$ ,  $S_1$ ,  $S_0$ , the register whose LD control input must be active (if any), a memory read/write operation (if required) and the operation in adder and logic circuit (if any) in the tabular format as shown in Table II:
  - $PC \leftarrow AR$
  - $M[AR] \leftarrow DR$
  - $AC \leftarrow AC + M[AR]$

- Which instruction is required to transfer the control from main program to an I/O program located at memory address  $X$ ? Which instruction is required at the end of an I/O program to transfer the control back to an address  $Y$  where return address is stored?